ANNEXE 2

Capteurs Pt100 Ω

La relation entre la résistance et la température, ainsi que les tolérances, sont définies dans les Normes européennes IEC 751.

On distingue deux technologies :

- **résistances à fil de platine enroulé sur support isolant.** Ce support est dans la plupart des cas un corps céramique, mais il existe des supports en verre. Les domaines d'utilisation vont jusqu'à 450°C, exceptionnellement jusqu'à 850°C. Ces éléments sensibles sont utilisés pour leur grande exactitude et grande stabilité.
- **dépôt sur un substrat céramique d'un film de platine.** Les domaines d'utilisation vont jusqu'à 450°C. Leur stabilité est moindre par rapport aux éléments traditionnels à enroulement, mais elles ont une excellente tenue à la vibration jusqu'à 200°C, un temps de réponse plus court, et un coût plus faible.

D'autres matériaux disposent de lois caractéristiques de la température : Cuivre et Nickel (utilisation de moins en moins fréquente).

Table de correspondance IEC 751 (extraits) : température et résistance

°C EIT 90	Ω	°C EIT 90	Ω	C EIT 90	Ω	°C EIT 90	Ω	°C EIT 90	Ω
-200	18,52	10	103,90	210	179,53	410	250,53	610	316,92
-190	22,83	20	107,79	220	183,19	420	253,96	620	320,12
-180	27,10	30	111,67	230	186,84	430	257,38	630	323,30
-170	31,34	40	115,54	240	190,47	440	260,78	640	326,48
-160	35,54	50	119,40	250	194,10	450	264,18	650	329,64
-150	39,72	60	123,24	260	197,71	460	267,56	660	332,79
-140	43,88	70	127,08	270	201,31	470	270,93	670	335,93
-130	48,00	80	130,90	280	204,90	480	274,29	680	339,06
-120	52,11	90	134,71	290	208,48	490	277,64	690	342,18
-110	56,19	100	138,51	300	212,05	500	280,98	700	345,28
-100	60,26	110	142,29	310	215,61	510	284,30	710	348,38
-90	64,30	120	146,07	320	219,15	520	287,62	720	351,46
-80	68,33	130	149,83	330	222,68	530	290,92	730	354,53
-70	72,33	140	153,58	340	226,21	540	294,21	740	357,59
-60	76,33	150	157,33	350	229,72	550	297,49	750	360,64
-50	80,31	160	161,05	360	233,21	560	300,75	760	363,67
-40	84,27	170	164,77	370	236,70	570	304,01	770	366,70
-30	88,22	180	168,48	380	240,18	580	307,25	780	369,71
-20	92,16	190	172,17	390	243,64	590	310,49	790	372,71
-10	96,09	200	175,86	400	247,09	600	313,71	800	375,70
0	100,00							810	378,68
								820	381,65
								830	384,60
								840	387,55
								850	390,48

La résistance en Pt peut être approximée par la relation :

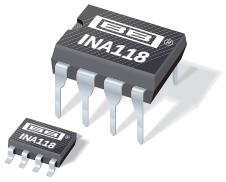
$$R_T = R_0 (1 + aT + bT^{2)}$$

Coéficients	Valeur
a	$3{,}9083 \times 10^{-3}$
b	$-5{,}775 \times 10^{-7}$

$R_0 = 100\Omega$ à 0°C

D'après la Norme, la classe de tolérance A ne peut pas être appliquée aux thermomètres exposés à des températures supérieures à 650°C.
Selon notre expérience nous limitons les capteurs industriels Pt100 Ω à 450°C pour ce qui concerne la Classe A.

BURR-BROWN®



ANNEXE 3

INA118

Precision, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.5μV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±1.35 to ±18V
- LOW QUIESCENT CURRENT: 350μA
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

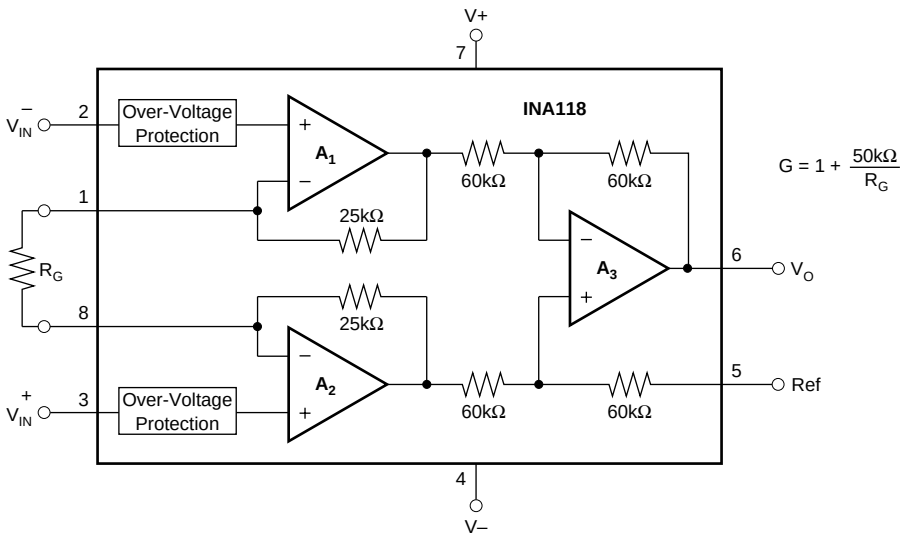
DESCRIPTION

The INA118 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (70kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA118 is laser trimmed for very low offset voltage (50μV), drift (0.5μV/°C) and high common-mode rejection (110dB at G = 1000). It operates with power supplies as low as ±1.35V, and quiescent current is only 350μA—ideal for battery operated systems.

The INA118 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

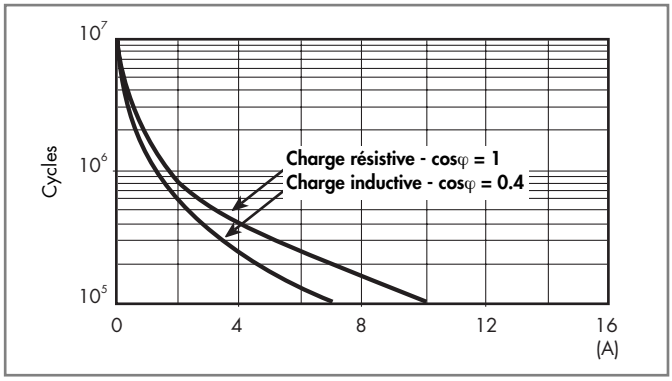
Printed in U.S.A. April, 1998

finder

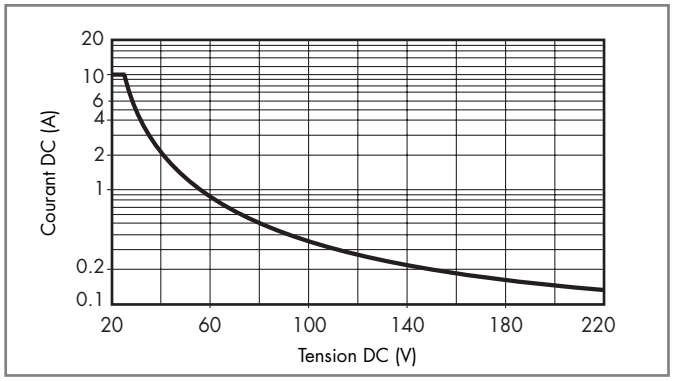
Série 36 - Relais miniatures pour circuit imprimé 10 A

Caractéristiques des contacts

F 36 - Durée de vie électrique (AC) en fonction de la charge



H 36 - Pouvoir de coupure maxi pour une charge en DC1



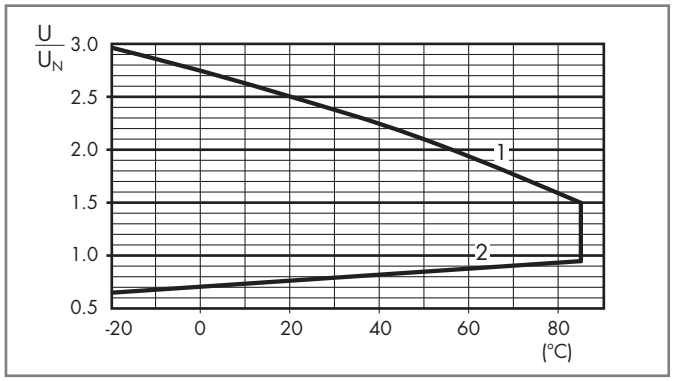
- La durée de vie électrique pour des charges résistives en DC1 ayant des valeurs de tension et de courant sous la courbe est ≥ 100x10³ cycles.
- Pour les charges en DC13, le raccordement d'une diode polarité inverse en parallèle avec la charge permet d'obtenir une durée de vie électrique identique à celle obtenue avec une charge en DC1. Nota: le temps de coupure de la charge sera augmenté.

Caractéristiques de la bobine

Données version DC

Tension nominale U_N	Code bobine	Plage de fonctionnement U_{min}	Plage de fonctionnement U_{max}	Résistance R	I nominale absorbée à U_N
V		V	V	Ω	mA
3	**9**.003	2.2	4.5	25	120
5	**9**.005	3.7	7.5	70	72
6	**9**.006	4.5	9	100	60
9	**9**.009	6.7	13.5	225	40
12	**9**.012	9	18	400	30
24	**9**.024	18	36	1600	15
48	**9**.048	36	72	6400	7.5

R 36 - Plage de fonctionnement bobine DC en fonction de la température ambiante



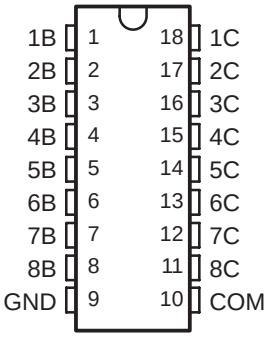
1 - Tension max admissible sur la bobine.
2 - Tension mini de fonctionnement avec la bobine à température ambiante.

ULN2803A
DARLINGTON TRANSISTOR ARRAY

SLRS049E − FEBRUARY1997 − REVISED JULY 2006

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Compatible with ULN2800A Series**

DW OR N PACKAGE
(TOP VIEW)

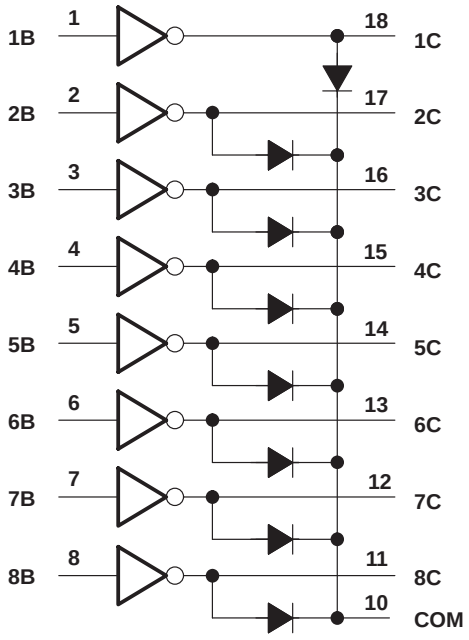


description/ordering information

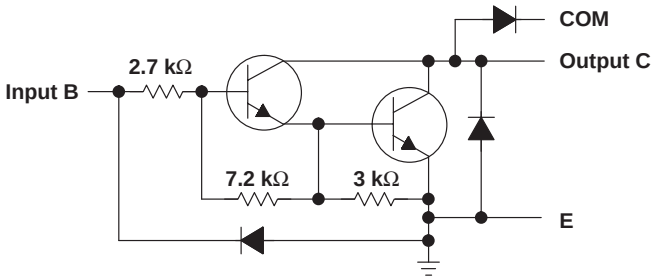
The ULN2803A is a high-voltage, high-current Darlington transistor array. The device consists of eight npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

logic diagram



schematic (each Darlington pair)



FAIRCHILD SEMICONDUCTOR™

November 1988
Revised June 2001

74AC377 • 74ACT377
Octal D-Type Flip-Flop with Clock Enable

General Description

The AC/ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

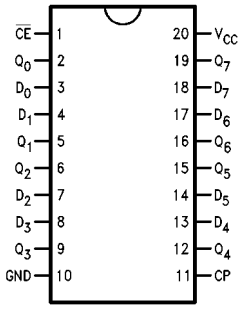
- I_{CC} reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See 273 for master reset version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- ACT377 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V_{CC} − 0.1V
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V_{CC} − 0.1V
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C922 • MM74C923
16-Key Encoder • 20-Key Encoder

General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

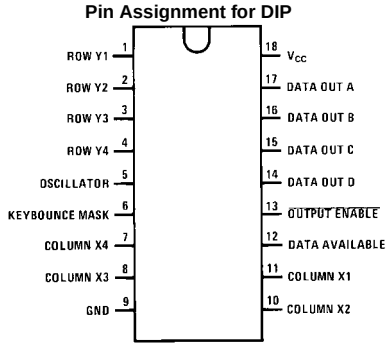
Ordering Code:

Order Number	Package Number	Package Description
MM74C922N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C922WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

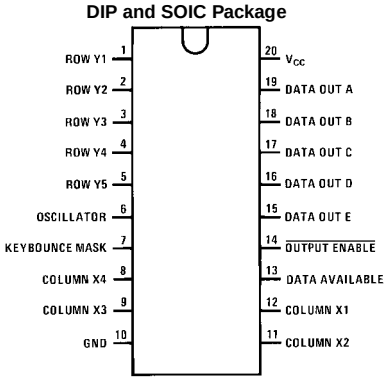
Connection Diagrams

Pin Assignment for DIP



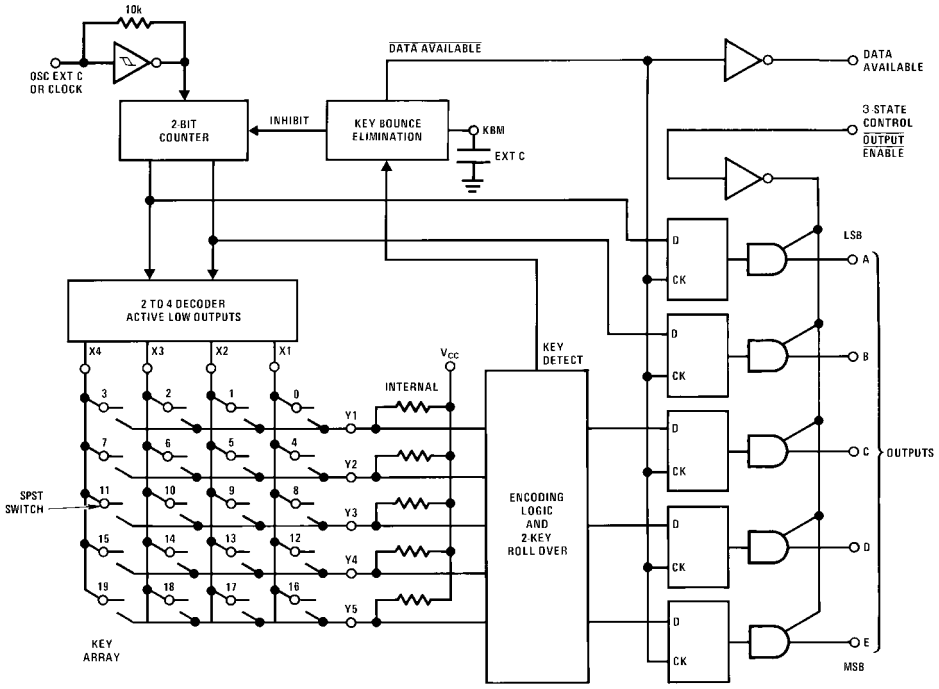
Top View
MM94C922

Pin Assignment for DIP and SOIC Package



Top View
MM74C923

Block Diagram



Truth Tables

(Pins 0 through 11)

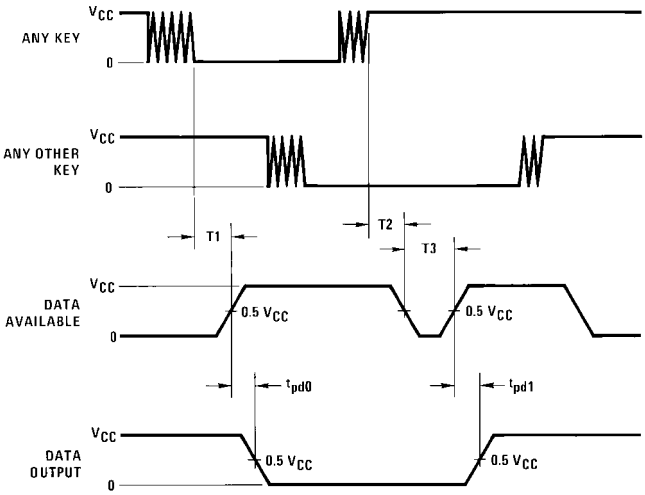
Switch Position		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4
DATA	A	0	1	0	1	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1	0	0	0	0
	D	0	0	0	0	0	0	0	0	1	1	1	1
	E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0

(Pins 12 through 19)

Switch Position		12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5(Note 1), X1	17 Y5 (Note 1), X2	18 Y5 (Note 1), X3	19 Y5 (Note 1), X4
DATA	A	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1
	C	1	1	1	1	0	0	0	0
	D	1	1	1	1	0	0	0	0
	E (Note 1)	0	0	0	0	1	1	1	1

Note 1: Omit for MM74C922

Switching Time Waveforms

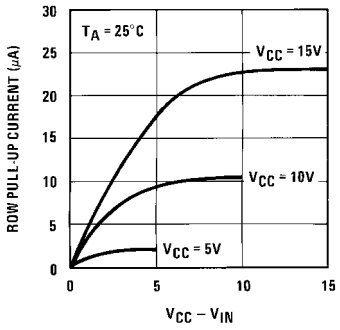


T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC, where R ≈ 10k and C is external capacitor at KBM input.

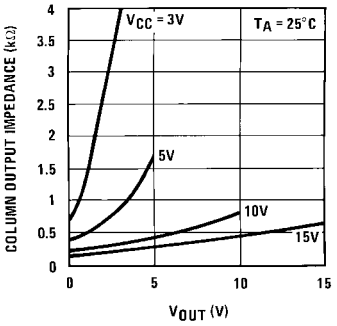
FIGURE 1.

Typical Performance Characteristics

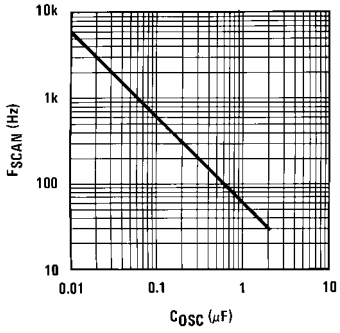
Typical I_{rp} vs V_{IN} at Any Y Input



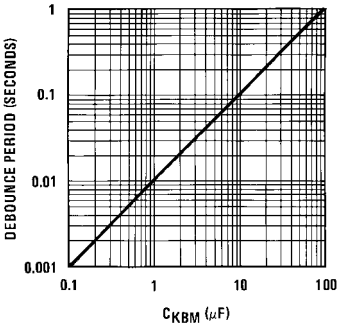
Typical R_{on} vs V_{OUT} at Any X Output



Typical F_{SCAN} vs C_{OSC}

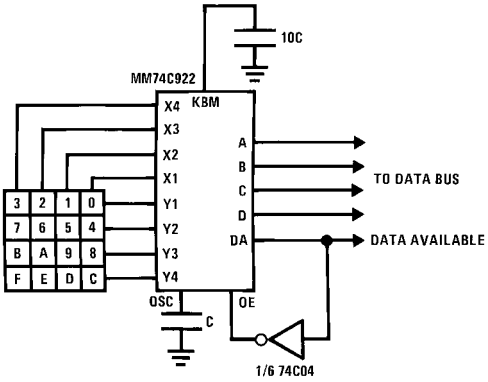


Typical Debounce Period vs C_{KBM}



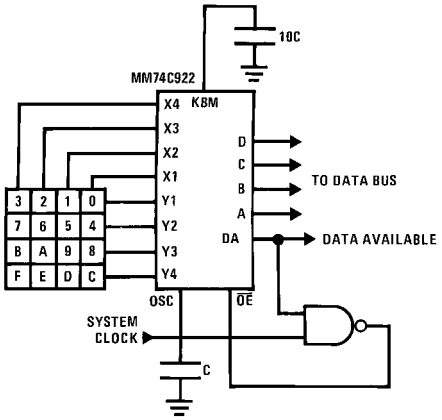
Typical Applications

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed 3-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

ANALOG DEVICES

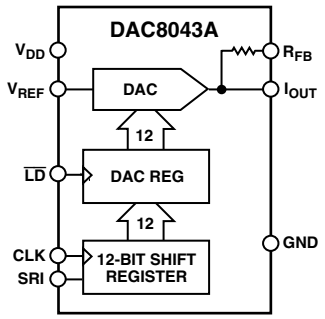
12-Bit Serial Input Multiplying D/A Converter

DAC8043A

FEATURES
Compact SOIC, and TSSOP Packages
True 12-Bit Accuracy
5 V Operation @ <10 μA
Fast 3-Wire Serial Input
Fast 1 μs Settling Time
2.4 MHz 4-Quadrant Multiply BW
Pin-for-Pin Upgrade for DAC8043
Standard and Rotated Pinout

APPLICATIONS
Ideal for PLC Applications in Industrial Control
Programmable Amplifiers and Attenuators
Digitally Controlled Calibration and Filters
Motion Control Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC8043A is an improved high accuracy 12-bit multiplying digital-to-analog converter in space-saving 8-lead packages. Featuring serial input, double buffering and excellent analog performance, the DAC8043A is ideal for applications where PC board space is at a premium. Improved linearity and gain error performance permit reduced parts count through the elimination of trimming components. Separate input clock and load DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in/parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin. Data in the DAC register is converted to an output current by the D/A converter.

Consuming only 10 μA from a single 5 V power supply, the DAC8043A is the ideal low power, small size, high performance solution to many application problems.

The DAC8043A is specified over the extended industrial (–40°C to +85°C) temperature range. DAC8043A is available in a PDIP package, and the low profile 1.75 mm height SOIC-8 surface mount packages. The DAC8043AFRU is available for ultra-compact applications in a thin 1.1 mm TSSOP-8 package.

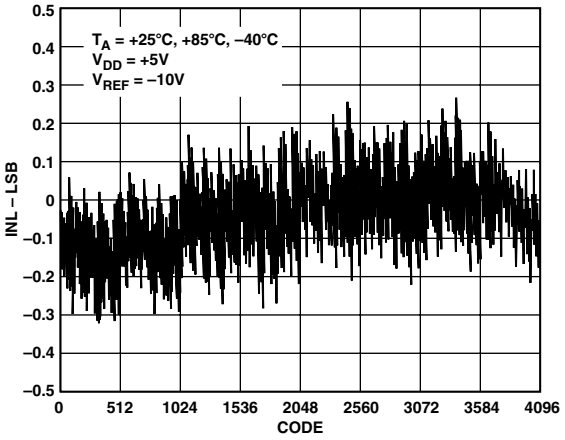


Figure 1. Integral Nonlinearity Error vs. Code

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/461-3113

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . –0.3 V, +8 V
V_{REF} to GND . . . . . ±18 V
R_{FB} to GND . . . . . ±18 V
Logic Inputs to GND . . . . . –0.3 V, V_{DD} + 0.3 V
VI_{OUT} to GND . . . . . –0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND . . . . . 50 mA
Package Power Dissipation . . . . . $(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
8-Lead PDIP Package (N-8) . . . . . 103°C/W
8-Lead SOIC Package (R-8) . . . . . 158°C/W
8-Lead TSSOP Package (RU-8) . . . . . 240°C/W
Maximum Junction Temperature (T_J max) . . . . . 150°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION DESCRIPTIONS

#(*)	Name	Function
1(7)	V_{REF}	DAC Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
2 (8)	R_{FB}	Internal Matching Feedback Resistor. Connect to external op amp output.
3 (1)	I_{OUT}	DAC Current Output, full-scale output 1 LSB less than reference input voltage $-V_{REF}$.
4 (2)	GND	Analog and Digital Ground.
5 (3)	$\overline{LD}$	Load Strobe, Level-Sensitive Digital Input. Transfers shift-register data to DAC register while active low. See truth table for operation.
6 (4)	SRI	12-Bit Serial Register Input, data loads directly into the shift register MSB first. Extra leading bits are ignored.
7 (5)	CLK	Clock Input, positive-edge clocks data into shift register.
8 (6)	V_{DD}	Positive Power Supply Input. Specified range of operation 5 V ± 10%.

*Note Pin numbers in parenthesis represent the rotated pinout of the DAC8043A1ES and DAC8043A1FS models.

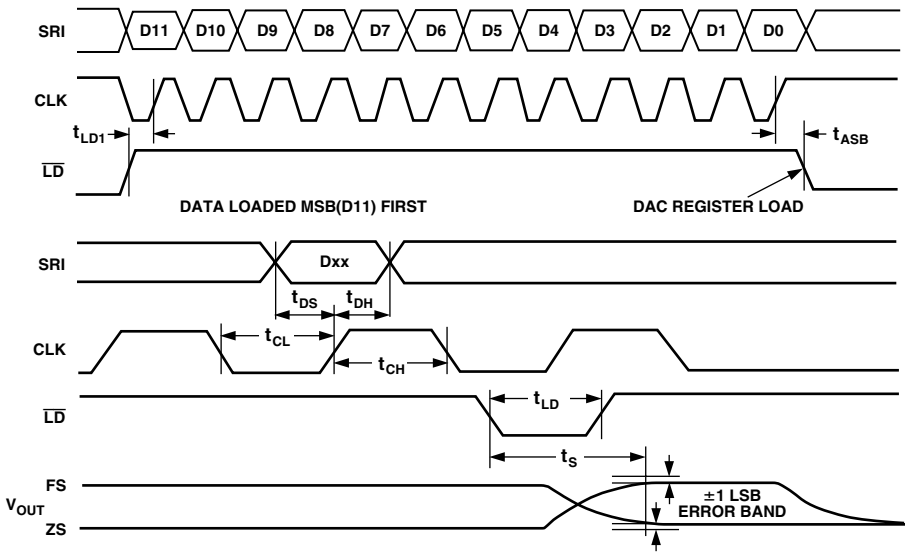


Figure 2. Timing Diagram

Table I. Control-Logic Truth Table

CLK	$\overline{LD}$	Serial Shift Register Function	DAC Register Function
↑	H	Shift-Register-Data Advanced One Bit	Latched
H or L	L	No Effect	Updated with Current Shift Register Contents
L	↑	No Effect	Latched All 12 Bits

NOTES
↑ positive logic transition.
The DAC Register $\overline{LD}$ input is level-sensitive. Any time $\overline{LD}$ is logic-low data in the serial register will directly control the switches in the R-2R DAC ladder.